CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of operating a pixel of an image sensor comprising:

accumulating charge in a photosensor;

transferring said charge from said photosensor to a storage device;

transferring said charge from said storage device to a floating diffusion node; and

reading out the charge residing in said floating diffusion node.

2. The method of claim 1, wherein said storage device comprises a storage element residing above a substrate containing said pixel and a storage node within said substrate.

3. A method of operating a plurality of pixels of an image sensor comprising:

accumulating a first charge in a first photosensor;

transferring said first charge from said first photosensor to a first storage device;

transferring said first charge from said first storage device to a floating diffusion node;

reading out the first charge from said floating diffusion node;

accumulating a second charge in a second photosensor;

transferring said second charge from said second photosensor to a second storage device;

transferring said second charge from said second storage device to said floating diffusion node; and

reading out the second charge from said floating diffusion node.

4. The method of claim 3, wherein a portion of said first and second storage devices reside above a substrate in which the first and second photosensors reside.

5. The method of claim 3 further comprising the act of sharing said floating diffusion node with a third and fourth pixel, wherein said floating diffusion node is reset, said third pixel accumulates a third charge in a third photosensor, transfers said third charge from said third photosensor to a third storage device, transfers said third charge from said third storage device to said floating diffusion node and reads out the third charge from said floating diffusion node; and

wherein said floating diffusion node is reset, said fourth pixel accumulates a fourth charge in a fourth photosensor, transfers said fourth charge from said fourth photosensor to a fourth storage device, transfers said fourth charge from said fourth storage device to said floating diffusion node and reads out the fourth charge from said floating diffusion node.

6. The method of claim 3, wherein a readout circuit outputs the first and second charges by: turning on a first transfer gate of a first pixel to transfer the first charge to the floating diffusion node, and turning on a row select transistor; and

turning on a second transfer gate of a second pixel after the readout of said first pixel to transfer the second charge to said floating diffusion node, and turning on said row select transistor.

7. The method of claim 6, wherein said transferring steps occur on half clock cycles.

8. A method of reading charge from pixels of an image sensor comprising:

turning on a first transfer gate transistor associated with a first pixel to transfer a first charge to a floating diffusion node;

turning on a row select transistor connected to the floating diffusion node to output the first charge from said floating diffusion node; and

while the row select transistor remains on, turning on a second transfer gate transistor associated with a second pixel to transfer a second charge to said floating diffusion node and to output the second charge from said floating diffusion node.

9. The method of claim 8, wherein the transfer of said first and second charges occur on a respective half clock cycle.

10. The method of claim 8, wherein said first transfer gate remains on during an integration period.

11. A pixel circuit for use in an imaging device, said pixel circuit comprising:

a photosensor for generating charge during an integration period;

a shutter transistor connected to said photosensor to transfer charge from said photosensor;

a storage capacitor connected to said shutter transistor to receive said charge transferred by said shutter transistor;

a transfer gate connected to said storage capacitor to transfer charge from said storage capacitor;

a floating diffusion node connected to said transfer gate to receive said charge from said transfer gate; and

a readout circuit connected to said floating diffusion node to output the charge accumulated at the floating diffusion node.

12. The circuit of claim 11, wherein said readout circuit further comprises:

a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node;

a source-follower transistor connected to said reset transistor for receiving charge from the floating diffusion node; and

a row select transistor connected to said source-follower transistor for outputting a signal produced by said source follower transistor.

13. The circuit of claim 11, wherein said capacitor is formed above a substrate in which the floating diffusion node is formed.

14. The circuit of claim 13, wherein said capacitor is a polypropylene capacitor.

15. The circuit of claim 11, wherein said shutter transistor is an electronic shutter for said pixel.

16. The circuit of claim 11, wherein said shutter transistor remains on during the integration period.

17. The circuit of claim 11, wherein said pixel is a CMOS pixel.

18. The circuit of claim 11, wherein said pixel comprises five transistors.

19. A pixel circuit for use in an imaging device, said pixel circuit comprising:

a plurality of photosensors for generating charge during an integration period;

a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor;

a plurality of storage nodes, each node coupled to a respective shutter transistor and storing charge transferred by a respective one of said plurality of photosensors;

a plurality of transfer gates, each transfer gate connected to and transferring charge from a respective storage node;

a floating diffusion node connected to said plurality of transfer gates for receiving charge from said transfer gates; and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node.

20. The circuit of claim 19 wherein said readout circuit further comprises a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node prior to receiving charge from a respective one said plurality of transfer gates.

21. The circuit of claim 19, wherein said storage nodes comprise capacitors formed above a substrate in which the floating diffusion node is formed.

22. The circuit of claim 21, wherein said capacitors are polypropylene capacitors.

23. The circuit of claim 19, wherein said shutter transistors operate as electronic shutters for said pixel.

24. The circuit of claim 19, wherein said shutter transistors remain on during the integration period.

25. The circuit of claim 19, wherein said pixel is a CMOS pixel.

26. The circuit of claim 19, wherein said pixel is a five transistor pixel.

27. A pixel circuit for use in an imaging device, said pixel circuit comprising:

a photosensor for generating charge during an integration period;

a shutter transistor connected to said photosensor to transfer charge from said photosensor;

a storage capacitor connected to said shutter transistor to receive said charge transferred by said shutter transistor;

a transfer gate connected to said storage capacitor to transfer charge from said storage capacitor;

a floating diffusion node connected to said transfer gate to receive said charge from said transfer gate;

a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node;

a source-follower transistor connected to said reset transistor for receiving charge from the floating diffusion node; and

a row select transistor connected to said source-follower transistor for outputting a signal produced by said source follower transistor.

28. The circuit of claim 27, wherein a plurality of pixel circuits share said floating diffusion node, reset transistor, source follower transistor, and row select transistor.

29. The circuit of claim 27, wherein said pixel is a CMOS pixel.

30. A pixel sensor array comprising:

a plurality of pixels, each pixel comprising:

a photosensor for generating charge during an integration period;

a shutter transistor connected to said photosensor to transfer charge from said photosensor;

a storage capacitor connected to said shutter transistor to receive said charge transferred by said shutter transistor;

a transfer gate connected to said storage capacitor to transfer charge from said storage capacitor;

a floating diffusion node connected to said transfer gate to receive said charge from said transfer gate; and

a readout circuit connected to said floating diffusion node to output the charge accumulated at the floating diffusion node.

31. The array of claim 30 wherein said readout circuit further comprises a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node.

32. The array of claim 30, wherein said capacitor is formed above a substrate in which the floating diffusion node is formed.

33. The array of claim 30, wherein said shutter transistor is an electronic shutter.

34. The array of claim 30, wherein the shutter transistor remains on during an integration period.

35. The array of claim 30, wherein said pixel is a CMOS pixel.

36. An imaging system pixel comprising:

a processor; and

an imaging device comprising an array of pixels, coupled to said imaging system comprising:

a photosensor for generating charge during an integration period;

a shutter transistor connected to said photosensor to transfer charge from said photosensor;

a storage capacitor connected to said shutter transistor to receive said charge transferred by said shutter transistor;

a transfer gate connected to said storage capacitor to transfer charge from said storage capacitor;

a floating diffusion node connected to said transfer gate to receive said charge from said transfer gate; and

a readout circuit connected to said floating diffusion node to output the charge accumulated at the floating diffusion node.

37. The system of claim 36, wherein said capacitor is formed above a substrate in which the floating diffusion node is formed.

38. The system of claim 37, wherein said capacitor is a polypropylene capacitor.

39. The system of claim 36, wherein said shutter transistor is an electronic shutter.

40. The system of claim 36, wherein said shutter transistor remains on during the integration period.

41. The system of claim 36, wherein said imaging system is a CMOS imaging system.

42. An imaging system comprising:

a processor; and

an imaging device comprising an array of pixels, coupled to said imaging system comprising:

a plurality of photosensors for generating charge during an integration period;

a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor;

a plurality of storage capacitors, each capacitor coupled to a respective shutter transistor and storing charge transferred by a respective one of said plurality of photosensors;

a plurality of transfer gates, each transfer gate connected to and transferring charge from a respective storage capacitor;

a floating diffusion node connected to said plurality of transfer gates for receiving charge from said transfer gates; and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node.

43. The system of claim 42, wherein a number of said plurality of photosensors is two photosensors.

44. The system of claim 42, wherein a number of said plurality of photosensors is four photosensors.

45. The system of claim 42, wherein said shutter transistor is an electronic shutter.

46. The system of claim 42, wherein said shutter transistor remains on during the integration period.

47. The system of claim 42, wherein said capacitors are polypropylene capacitors.

48. The system of claim 42, wherein said imaging system is a CMOS imaging system.